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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,309	09/12/2005	Joon-Hoo Choi	PANK91700 US	1450

90323 7590 08/05/2010

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EXAMINER	
SALERNO, SARAH KATE	
ART UNIT	PAPER NUMBER
2814	

MAIL DATE	DELIVERY MODE
08/05/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/521,309	CHOI ET AL.	
	Examiner	Art Unit	
	SARAH K. SALERNO	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 10-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 10-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/26/10 has been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 4, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin (KR 10-2002-0078535), in view of Hwang et al. (US PGPub 2002/0158995) and Kimura (US PGPub 2003/0170944).

Claim1: Shin teaches an organic EL display panel comprising (FIG. 6): an substrate (110); a polysilicon layer disposed on the substrate (130); a gate insulating layer (140) disposed on the polysilicon layer; a gate wire (150) disposed on the gate insulating layer; an interlayer insulating film (160) disposed on the gate wire; a data wire (170) disposed on the interlayer insulating film; a pixel electrode (200) disposed on the

same layer (140) as the data wire; an organic EL layer (220) disposed on the pixel electrode and defining a predetermined area; a partition (210) disposed on the data wire and directly disposed on the pixel electrode and defining the predetermined area; and a common electrode (230) disposed on the organic EL layer and the partition (Fig . 7).

Shin does not specify that the substrate is insulating of the pixel electrode contacts the polysilicon layer. Hwang teaches an insulating substrate (100) and a pixel electrode contacts (114b) the polysilicon layer (150s) as is known in the art to use for organic EL display devices and to reduce manufacturing steps and cost (Fig. 2; [0019-0022, 0052-0054]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Shin to specify the substrate being insulating as it is known in the art to use insulating substrates and for the pixel electrode to contact the polysilicon layer to reduce manufacturing steps and cost as taught by Hwang (Fig. 2; [0019-0022, 0052-0054]).

Shin and Hwang do not teach the partition formed directly on both the data wire and the pixel electrode. Kimura teaches the partition (4516) formed directly on both the data (source electrode) and the pixel electrode (4517) to flatten and pattern to enable EL layer formation (FIG. 13; [0198, 0199 & 0256). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Shin and Hwang to have the partition formed directly on both the data wire and the pixel electrode to flatten and pattern to enable EL layer formation as taught by Kimura (FIG. 13; [0198, 0199 & 0256).

It is noted that the claim language "a pixel electrode disposed on the same layer as the data wire" does not require the pixel and data wires to be formed directly on the same layer or being made of the same layer of material, therefore the layer that the pixel electrode and data wired are both disposed on is any layer that they are both on top of or below such as (140), as mentioned above, or (120), (110), etc.

Claim 2: Shin teaches the pixel electrode includes the same material as the data wire (Page 3).

Claim 4 and 11: Shin teaches a buffer layer (235) disposed between the organic EL layer and the common electrode.

3. Claims 3, 6, 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin (KR 10-2002-0078535), in view of Hwang et al. (US PGPub 2002/0158995) and Kimura (US PGPub 2003/0170944) as applied to claim 1 and 2, above and further in view of Yamazaki et al. (US PGPub 2001/0026125 of record).

Regarding claims 3 and 10, Shin, Hwang, and Kimura substantially read on the invention as claimed, except Shin, Hwang, and Kimura do not teach the polysilicon layer comprises first and second transistor portions including source regions and drain regions and a storage electrode portion connected to the second transistor portion, the gate wire comprises first and second gate electrodes and a storage electrode overlapping the first and the second transistor portions and the storage electrode portion, respectively, the data wire comprises first and second data lines, a first source electrode connected to the first data line and the source region of the first transistor

portion, a first drain electrode connected to the drain region the first transistor portion and the second gate electrode, and a second source electrode connected to the second data line and the source region of the second transistor portion, and the pixel electrode is connected to the drain region of the second transistor. Yamazaki teaches the polysilicon layer (13-17, 31-32 & 34) comprises first (601) and second transistor portions (602) including source regions (13, 36) and drain regions (14 & 32) and a storage electrode portion (51) connected to the second transistor portion (602), the gate wire comprises first (19a) and second (35) gate electrodes and a storage electrode (35) overlapping the first (601) and the second transistor (602) portions and the storage electrode portion (51), respectively, the data wire comprises first and second data lines, a first source electrode (21) connected to the first data line and the source region (13) of the first transistor portion (601), a first drain electrode (22) connected to the drain region (14) the first transistor portion (601) and the second gate electrode (35), and a second source electrode (36) connected to the second data line and the source region (31) of the second transistor portion (602), and the pixel electrode (40) is connected to the drain region (32) of the second transistor (602) for maintaining the voltage that is applied to the gate electrode of the current controlling TFT 602 and to create a high displaying quality (FIG. 6, 7A; [0078-0091]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Shin, Hwang, and Kimura to include the first and second transistors, the capacitor and their connections to maintain the controlling voltage and to create a high display quality as taught by Yamazaki (FIG. 6, 7A; [0078-0091]).

Claims 6 & 13: Yamazaki teaches an auxiliary electrode (41b) contacting the common electrode (44) (FIG. 6).

4. Claims 5 & 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin (KR 10-2002-0078535), Hwang et al. (US PGPub 2002/0158995), and Kimura (US PGPub 2003/0170944), as applied to claims 1 & 2 above, and further in view of Yamazaki et al. (US Patent 6,013,930).

Regarding claims 5 & 12, as described above, Shin, Hwang, and Kimura substantially read on the invention as claimed, except Shin, Hwang, and Kimura do not teach the partition comprises black photoresist. Yamazaki teaches the use of a black photosensitive acrylic resin between pixel electrodes (Col. 25 lines 30-67) to produce a highly-reliable and highly reproducible device (col. 2 lines 23-30). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Shin, Hwang, and Kimura to make the acrylic resin a black photosensitive acrylic resin to produce a highly-reliable and highly reproducible device as taught by Yamazaki (Col. 2 lines 23-30).

Response to Arguments

5. Applicant's arguments with respect to claims 1-6 and 10-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SARAH K. SALERNO whose telephone number is (571)270-1266. The examiner can normally be reached on M-R 8:00-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wael M Fahmy/
Supervisory Patent Examiner, Art Unit 2814

/S. K. S./
Examiner, Art Unit 2814